pB10A

The convenient small hand held bench top 10 Gb/s CDR, BERT and Clock Synthesis Unit

Features

- Data rates from 9.95 Gb/s to 11.35 Gb/s
- Recovers clock and data from incoming serial data stream
- Integrated pattern generator provides PRBS 2^{31}–1, 2^{23}–1, 2^{7}–1, and custom serial output patterns
- Build in PRBS Checker and BER counter/ calculator
- Programmable internal clock synthesizer
- Complies with XFP MSA standards
- 0°C to 50°C temperature range
- 1000 V ESD rating
- Small sized hand held bench top device (105 mm*144 mm*33 mm)
- Configuration and management via GUI interface to PC and API interface to access data fields in the GUI
- Powered by USB port or wall mount power supply

Transmitter Features

- Serial data output 9.95 to 11.35 Gb/s (CML)
- At rate serial transmitter clock output (CML)
- De-emphasis
- High/Low swing
- Polarity inverter

Receiver Features

- Single-Ended or Differential inputs
- Continuous 9.95 to 11.35 Gb/s data rates
- 20 mV input sensitivity
- EDC controls
- Lock Detect Indicator
- P_k-P_k voltage meter
- Polarity inverter

Clock Synthesizer Features

- 10 MHz to 760 MHz continuously programmable clock output (CML)

Description

The pB10A is a fully integrated 10 Gb/s CDR unit with serial 10 GHz clock output and PRBS generator/checker and BER calculator unit. The unit recovers SONET STS192 and 10 Gb/s Ethernet/ Fiber Channel clock and data streams in the entire data range from 9.95 Gb/s to 11.32 Gb/s. The build-in PRBS generator and checker enable the unit to test the BER of an electrical or optical link.

There is no need for an external reference clock as the unit uses an internal programmable clock generator. If needed an external reference clock can be applied.
The unit can also be used as a standalone precision wide range frequency source. It covers the range from 10 MHz to 760 MHz.

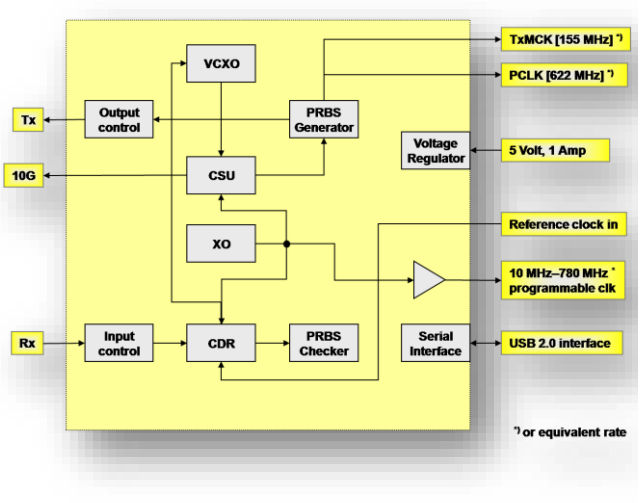
CDR mode

The pB10A receives a serial 10 Gb/s data stream from an O/E converter (APD or PIN) or any other electrical source and recovers clock and data. Typical applications are to extract the 10G clock while testing e.g. optical modules or other electrical PHY components where the testing equipment requires a recovered clock.

BIST mode

The pB10A has the capability to generate and check various 10 Gb/s PRBS patterns (2^{31}–1, 2^{23}–1, 2^{7}-1 and custom defined). In this mode the unit can be used to evaluate 10 Gb/s components or links with or without XFP, SFP modules. Provides a cost-effective source to generate non synchronized 10 Gb/s traffic e.g. for DWDM test beds.

pB10A block diagram:



CDR mode

The pB10A receives a serial 10 Gb/s data stream from an O/E converter (APD or PIN) or any other electrical source and recovers clock and data in the 9.95 Gb/s to 11.35 Gb/s data range. The device has high input sensitivity of 20 mV and covers a range up to a max. of 1.4 Volt input swing levels. The recovered clock (divided by 16 and 64) is externally available for further use. If needed an external reference clock can be provided to the CDR. In this case next to the divide by 16 and 64 there is also the possibility to feed a divide by 66 reference frequencies.

BIST mode

The pB10A has the capability to generate and check various 10 Gb/s PRBS patterns; 2^{31}–1, 2^{23}–1, 2^{7}-1, and custom defined. In this mode the unit can be used to evaluate 10 Gb/s components or links with or without XFP, SFP modules. On the receive path the incoming data stream is recovered and analyzed in the PRBS checker. BER values are read, calculated and displayed in the GUI.

Provides a cost-effective source to generate non synchronized 10 Gb/s traffic e.g. for DWDM test beds (see figure 5).

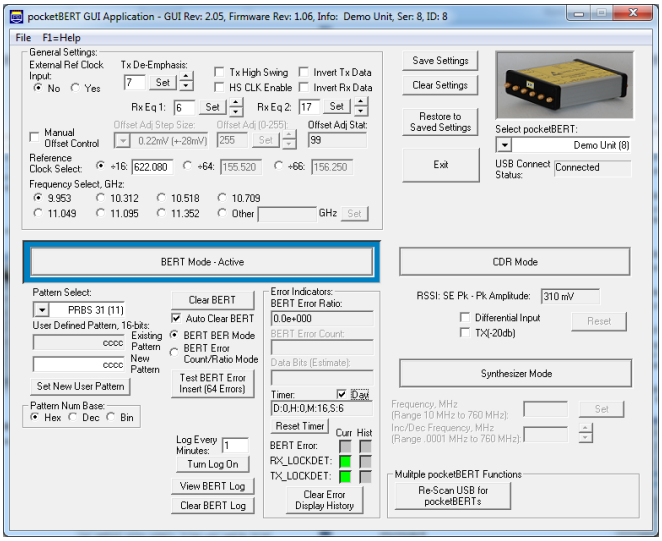
Clock Synthesizer Mode

With all CDR/PRBS features disabled the pB10A unit can be used as any-rate programmable clock source from 10 MHz to 760 MHz.

GUI Interface

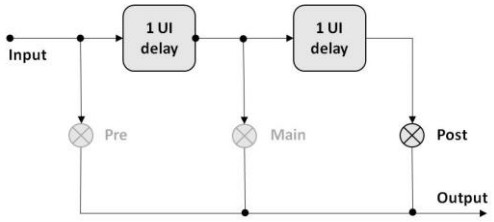
The Graphical User Interface (GUI) software controls the pB10A. The software runs on a PC/Laptop and uses a USB 2.0 interface to communicate with the pB10A. The software runs on the Windows operating systems.
The GUI selects one of three modes:

- BERT Mode
- CDR Mode
- Clock Synthesizer Mode

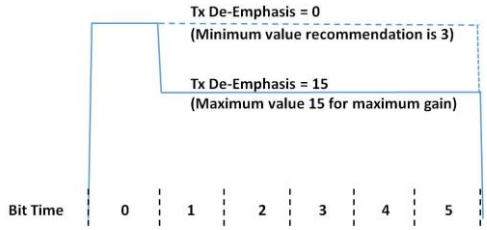


Tx De-Emphasis control

Tx De-emphasis control allows to compensate for imperfections of the transmit channel's impulse response and reduce the inter-symbol-interference (ISI). A 3 tap FIR filter controls the Tx P/N outputs.



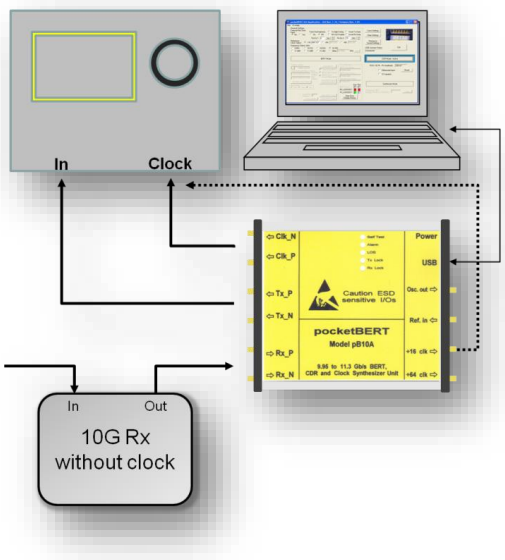
The Pre and Main Tap are factory set and the user has control over the Post-tap to optimize signal fidelity in his transmission path.



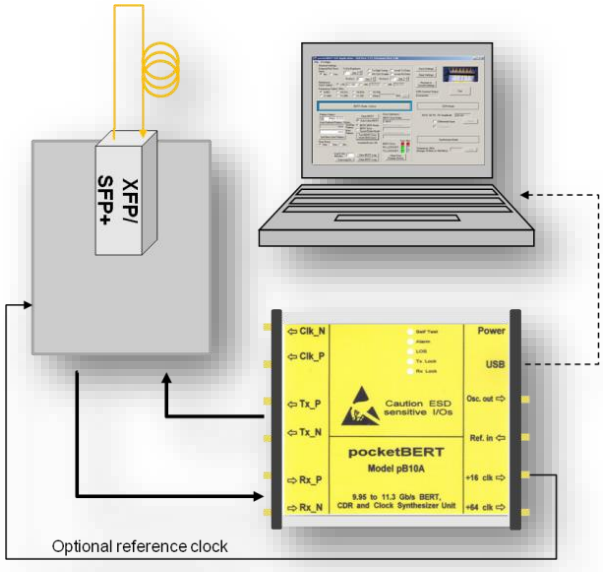
Receiver Equalizations
RxEq 1: Post-Amp Equalization controls a 2 tap FFE for pre-cursor response. It equalizes ISI caused by chromatic dispersion.
RxEq 2: controls linear equalization which provides peaking gain at 5.5 GHz. It equalizes ISI caused by FR-4 dispersion.

p10A Application Diagrams

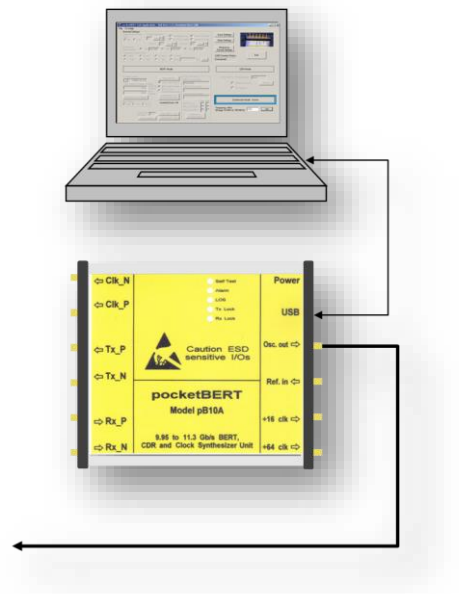
CDR mode:



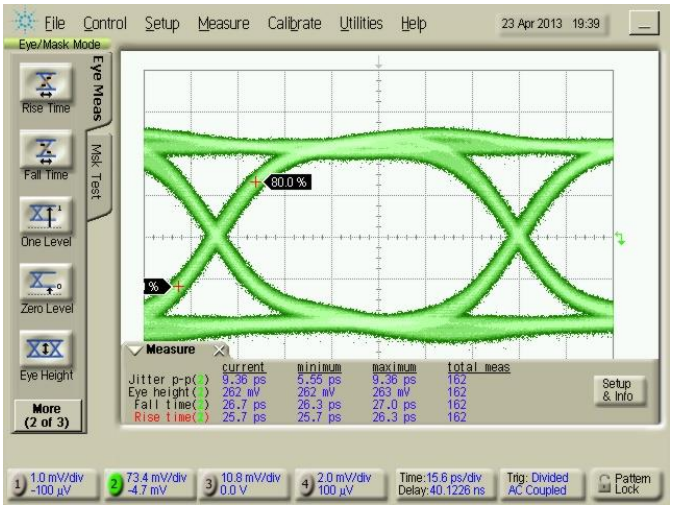
BERT Mode



Frequency Synthesizer Mode



Output Eye Diagram at 9.95 Gb/s



Dimensions:

Ordering information	pB10A
Availability	in Production

Please contact support@pocketbert.com for any commercial and technical questions.