pB100A4

Pocket size Quad 24 Gb/s - 30 Gb/s PRBS Generator and Checker, Bit Error Rate Tester (BERT)

Features

- Preset four-lane rate support for:
- 100GBASE-R4 at 25.78125 Gb/s
- OTL4 at 27.95 Gb/s
- 128G Fiber Channel at 28.05 Gb/s
- 24–30 Gb/s customer prog. data rates
- Configuration and management via GUI, Ethernet or API interface to PC, Error logs
- Affordable, small and universal quad 25, 27 and 28 Gb/s test gear
- Differential I/Os
- Customizable cable length
- Approx. size: 7” × 5” × 2”
- 15 watt typical power dissipation

Transmitter Features

- Tx Buffer pre- and post-cursor emphasis (0-7 dB)
- Programmable 28 Gb/s output voltage up to 1,000 mV_{ppd}
- PRBS generators 2^{31}–1, 2^{23}–1, 2^{15}-1 2^{9}-1, 2^{7}-1, Square wave, SSPR (OIF-CEI-03.0) and 128 Bit User Pattern

Receiver Features

- 40 mV_{ppd} minimum input sensitivity at 28 Gb/s
- Integrated peaking and limiting amplifier
- Internal 100 Ohm termination on differential CML inputs
- PRBS Checker
- Separate reporting on “0” and “1” error counts
- BER calculation
- Optional: eye monitoring capability

Clocking

- Integrated frequency synthesizer for standalone operation
- Extern clock input for synchronized applications
- Recovered clock and frequency synthesizer outputs

Description

The pB100A4 is a fully integrated quad 25.78125, 27.95 and 28.05 Gb/s PRBS generator and checker and BER calculator unit. The unit recovers 100GBASE-R4, OTL4 or 128 Gb/s fiber channel compliant data streams. The pB100A4 is controlled through an USB link to a PC. The Graphical User Interface (GUI) configures and controls the individual four data lanes to match the application specific setup for your electrical or optical links or components under test.
Each output and input can be adjusted individually for transmitter pre and post cursor emphasis and receiver peaking. Next to the standard PRBS patterns (2^{31}–1, 2^{23}–1, 2^{15}-1, 2^{9}-1, 2^{7}-1, Square wave (8-ones and 8-zeros)), a 128 bit custom defined pattern can be programmed.
There is no need for an external reference clock as the unit uses an internal programmable clock generator. If needed an external reference clock can be applied.

Ordering Information

Device	Description
pB100A4-SK12	Quad 28 Gb/s BERT, 12” H&S cable, SK-connector
pB100A4-SK24	Quad 28 Gb/s BERT, 24” H&S cable, SK-connector

Availability: in production
Price information: please contact info@pocketbert.com

pB100A4 Block Diagram

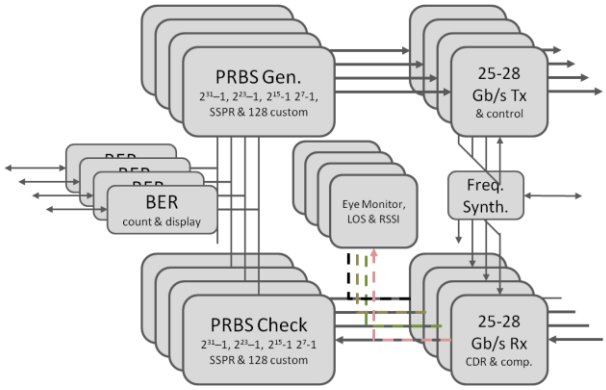


Figure 1: pB100A4 Block Diagram

pocketBERT operation

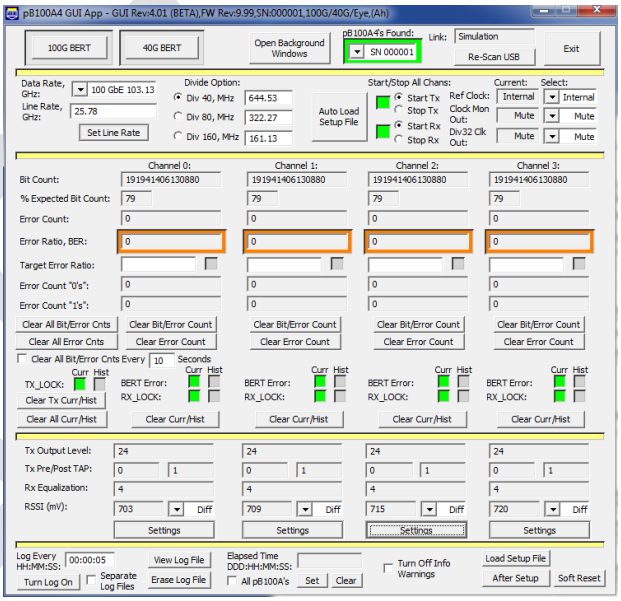
The pB100A4 has the capability to generate and check quad 25.78125, 27.95 and 28.05 Gb/s PRBS patterns. The build-in 4 individual PRBS generators and checkers will generate and analyze 2^{31}–1, 2^{23}–1, 2^{15}-1 2^{9}-1, 2^{7}-1, Square wave, SSPR (OIF-CEI-03.0) and 128 Bit User Patterns. The PRBS sequential start can be biased by individual "seed" settings. Internal frequency synthesizer will generate the required clocks for standalone operation. If needed, the unit can be driven by an external reference clock to run in synch with a test setup.

- Per lane de-/pre emphasis control for outputs
- Per lane output level control
- Per lane PRBS generator selection
- Per lane input equalization
- Per lane receive signal strength detection
- Per lane PRBS checker selection
- Per lane error reporting
- Per lane target BER settings
- Per lane clear/reset functions
- Per lane error insertion
- Per lane eye monitoring (optional)

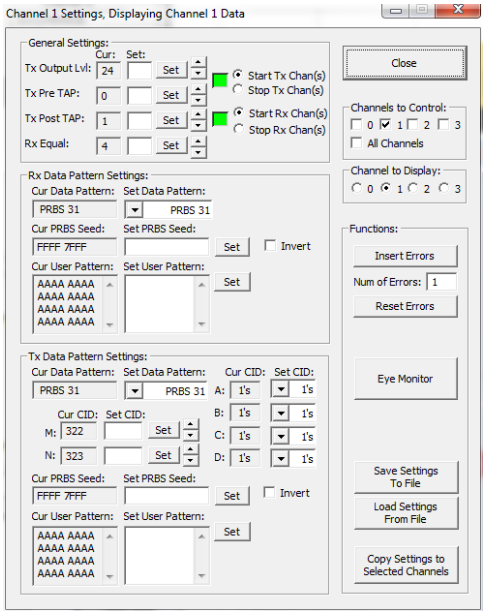
The unit can be used to evaluate 25, 27 or 28 Gb/s components or links. On the receive path the incoming data stream is recovered and analyzed in the PRBS checker. BER values and error counts on "0" and "1" are read, calculated and displayed in the GUI.

GUI Interface

The Graphical User Interface (GUI) software controls the 4 channels of pB100A4. The software runs on a PC/Laptop and uses a USB 2.0 interface to communicate with the pB100A4. The software runs on the Windows operating systems. Access to all GUI commands/read/write calls through an API interface enable easy integration to existing test apparatus. BERT log files are generated and can be read from the PC for further use.



Individual channel settings screen:



Each channel output amplitude can be set separately

Tx [0-3]:Output Level adjustment [Range:0–31]

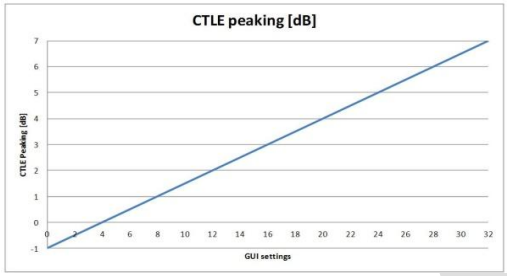
Tx [0-3] :FIR filter setting

Pre TAP [Range: 0 – 15]

Post TAP [Range: 0 – 15]

Rx [0-3] Equalization [Range: 0 – 31]

Rx [0-3] Eq: programmable continuous time linear equalization to compensate for channel impairments. At a setting of 0, the equalizer provides 0 dB peaking near 14 GHz.



Tx [0-3] Pattern Settings:

- PRBS 2^{31}-1
- PRBS 2^{23}-1
- PRBS 2^{15}-1
- PRBS 2^{9}-1
- PRBS 2^{7}-1
- SSPR
- CID (OIF-CEI-03.0)
- Square

2Hi/2Lo:

CCCC CCCC CCCC CCCC CCCC CCCC CCCC CCCC
CCCC CCCC CCCC CCCC CCCC CCCC CCCC CCCC

4Hi/4Lo:

F0F0 F0F0 F0F0 F0F0 F0F0 F0F0 F0F0 F0F0
F0F0 F0F0 F0F0 F0F0 F0F0 F0F0 F0F0 F0F0

8Hi/8Lo:

FF00 FF00 FF00 FF00 FF00 FF00 FF00 FF00
FF00 FF00 FF00 FF00 FF00 FF00 FF00 FF00

- **128 Bit User Pattern**: some restrictions may apply on the number of consecutive "0"s or "1"s based on the characteristics of the receiving CDR
- **Tx [0-3] Error Insertion**: single and multiple Errors [Range: 1 – 64]

CID pattern generation

A customizable consecutive identical digits (CID) test pattern may be enabled on any of the high speed lanes.

PRBS seeds

In addition, each lane has a 31 bit PRBS seed register that can be used to create different offsets for the PRBS patterns on each of the high speed lanes.

Insert Errors:

Up to 64 errors can be injected in the PRBS data stream with this command on the "selected" channels.

Clock-out [N/P]

Copy of the internally synthesized reference clock available in following divide ratios: div32, div40, div80 and div160. Differential signal can be used single ended, with 2nd leg terminated with 50 Ohm.

Reference Clock-in

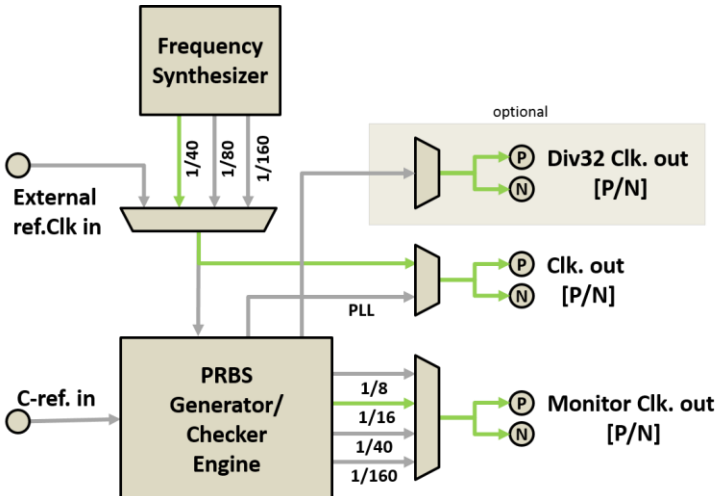
Ties the pB100A4 to an externally provided, single ended timing signal for the 24 Gb/s – 30 Gb/s line rates with div40, div80 and div160 options.

C-ref Clock-in

The single-ended c-reference clock input is an alternative reference source for the internal transmitter CMU clean-up PLL.

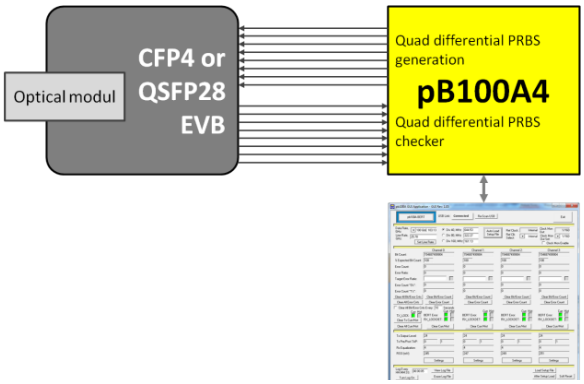
Monitor Clock-out [N/P]

Variety of clock ratios, derived from the recovered input receive signal: div8, div16, div32, div40, div80 and div160.

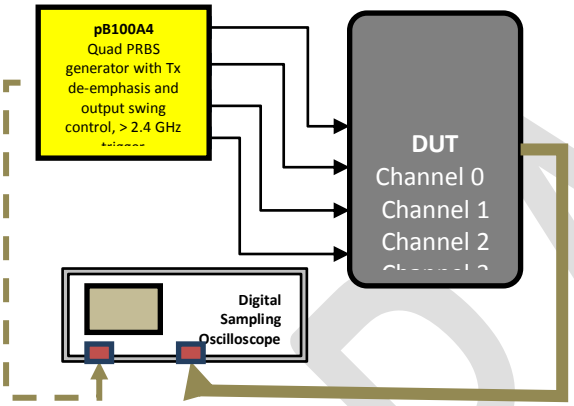


Application Diagrams

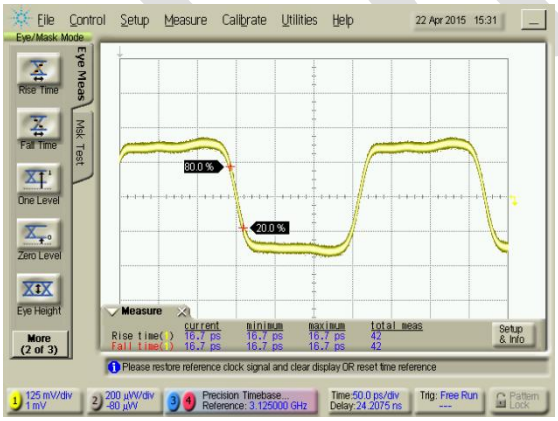
CFP4/QSFP28 testing



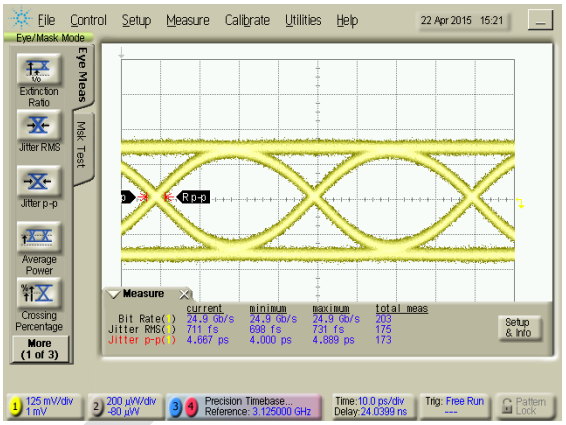
PRBS generation - precision time base trigger



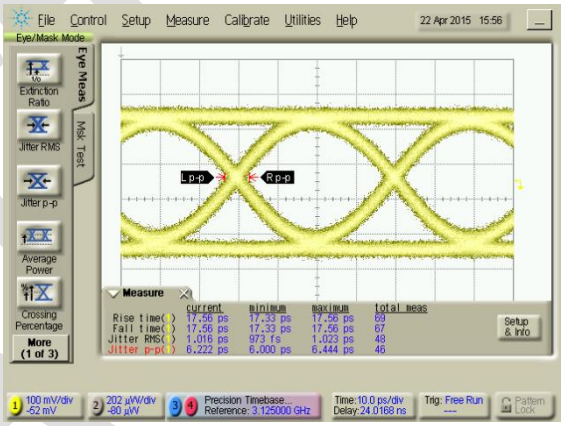
Typical Tr/Tf times



Output eye diagram 25 Gb/s



Output eye diagram 28 Gb/s



Dimensions: 7” × 5” × 2”, 2 lbs.

Optional features:

- Quad 8 – 12 Gb/s (pB40A4) operation
- Eye monitoring capability

Please contact support@pocketbert.com for any commercial and technical questions.